

## CLAIMS

1. A method for forming an NPN device and a vertical PNP device on a substrate, said method comprising steps of:

forming an insulating layer over an NPN region and a PNP region of said

5 substrate;

forming a buffer layer on said insulating layer;

forming an opening in said buffer layer and said insulating layer in said NPN region, said opening exposing said substrate;

forming a semiconductor layer on said buffer layer and in said opening, said  
10 semiconductor layer having a first portion situated in said opening in said NPN region and a second portion situated on said buffer layer in said PNP region;

wherein said first portion of said semiconductor layer forms a single crystal base of said NPN device and said second portion of said semiconductor layer forms a polycrystalline emitter of said vertical PNP device.

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2. The method of claim 1 further comprising a step of forming an emitter window opening in said insulating layer in said PNP region after said step of forming said insulating layer and before said step of forming said buffer layer.

20 3. The method of claim 1 wherein said semiconductor layer comprises silicon-germanium.

4. The method of claim 1 further comprising a step of forming an emitter of said NPN device over said single crystal base.

5. The method of claim 4 further comprising the steps of:  
5 forming extrinsic base regions of said NPN device in said semiconductor layer;  
simultaneously defining edges of said extrinsic base regions of said NPN device  
and edges of said polycrystalline emitter of said vertical PNP device.

6. The method of claim 1 wherein said insulating layer comprises TEOS  
10 oxide.

7. The method of claim 1 wherein said buffer layer comprises amorphous  
silicon.

15 8. A structure comprising:  
an insulating layer situated over an NPN region and a PNP region of a substrate;  
a buffer layer situated on said insulating layer;  
an opening in said buffer layer and said insulating layer in said NPN region, said  
opening exposing said substrate;  
20 a semiconductor layer situated on said buffer layer and in said opening, said  
semiconductor layer having a first portion situated in said opening and a second portion  
situated on said buffer layer in said PNP region;

wherein said first portion of said semiconductor layer forms a single crystal base of an NPN device and said second portion of said semiconductor layer forms a polycrystalline emitter of a vertical PNP device.

5           9.     The structure of claim 8 further comprising an emitter window opening in said insulating layer in said PNP region, said buffer layer being situated in said emitter window opening.

10           10.    The structure of claim 8 wherein said semiconductor layer comprises silicon-germanium.

11.    The structure of claim 8 further comprising an emitter of said NPN device, said emitter of said NPN device being situated over said single crystal base.

15           12.    The structure of claim 9 further comprising a interfacial oxide layer, said interfacial oxide layer being situated between said buffer layer and said substrate in said emitter window opening.

20           13.    The structure of claim 8 wherein said insulating layer comprises TEOS oxide.

14.    The structure of claim 8 wherein said buffer layer comprises amorphous

silicon.

15. A method for forming an NPN device and a vertical PNP device on a substrate, said method comprising steps of:

5 forming an insulating layer over an NPN region and a PNP region of said substrate;

forming a first opening in said insulating layer in said PNP region, said first opening exposing a first portion of said substrate;

forming a buffer layer on said insulating layer and in said first opening;

10 forming a second opening in said buffer layer and said insulating layer in said NPN region, said second opening exposing a second portion of said substrate;

forming a semiconductor layer on said buffer layer and in said second opening, said semiconductor layer having a first portion situated in said second opening and a second portion situated on said buffer layer in said PNP region;

15 wherein said first portion of said semiconductor layer forms a single crystal base of said NPN device and said second portion of said semiconductor layer forms a polycrystalline emitter of said vertical PNP device.

16. The method of claim 15 wherein said semiconductor layer comprises  
20 silicon-germanium.

17. The method of claim of claim 15 further comprising a step of forming an

emitter of said NPN device over said single crystal base.

18. The method of claim 17 further comprising the steps of:

forming extrinsic base regions of said NPN device in said semiconductor layer;

5 simultaneously defining edges of said extrinsic base regions of said NPN device

and edges of said polycrystalline emitter of said vertical PNP device.

19. The method of claim 15 wherein said insulating layer comprises TEOS  
oxide.

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20. The method of claim 15 wherein said buffer layer comprises amorphous  
silicon.